Effects of channel thickness variation on bias stress instability of InGaZnO thin-film transistors

Edward Namkyu Cho, Jung Han Kang, Ilgu Yun*

Department of Electrical and Electronic Engineering, 262 Seongsanno, Seodaemun-gu, Yonsei University, Seoul 120-749, Republic of Korea

A R T I C L E   I N F O

Article history:
Received 22 May 2011
Received in revised form 11 June 2011
Accepted 6 July 2011
Available online 29 July 2011

A B S T R A C T

Here, we report on the effects of channel (or active) layer thickness on the bias stress instability of InGaZnO (IGZO) thin-film transistors (TFTs). The investigation on variations of TFT characteristics under the electrical bias stress is very crucial for commercial applications. In this work, the initial electrical characteristics of the tested TFTs with different channel layer thicknesses (40, 50, and 60 nm) are performed. Various gate bias ($V_{GS}$) stresses (10, 20, and 30 V) are then applied to the tested TFTs. For all $V_{GS}$ stresses with different channel layer thickness, the experimentally measured threshold voltage shift ($\Delta V_{th}$) as a function of stress time is precisely modeled with stretched-exponential function. It is indicated that the $\Delta V_{th}$ is generated by carrier trapping but not defect creation. It is also observed that the $\Delta V_{th}$ shows incremental behavior as the channel layer thickness increases. Thus, it is verified that the increase of total trap states ($N_t$) and free carriers resulted in the increase of $\Delta V_{th}$ as the channel layer thickness increases.

1. Introduction

Transparent oxide thin film transistors (TFTs) are of great interest for the applications in flat-panel displays, optical sensors, and solar cells [1,2]. Recently, transparent oxide semiconductor based TFTs have attracted much attention for flexible displays because they can be fabricated on plastic substrates at low temperature and have the ability to be used to produce highly uniform and large area displays with a low production cost [1]. There has been an increase in research exploring effects of channel (or active) layer thickness on electrical characteristics of TFTs using oxide semiconductor materials such as ZnO [3], InZnO (IZO) [4], and InGaZnO (IGZO) [5]. In particular, IGZO TFTs have been rising to replace conventional a-Si TFTs due to high mobility and a reasonable on/off ratio [1,6]. However, like other TFTs, the characteristic variations of IGZO TFTs, such as the threshold voltage ($V_{th}$) variation, are occurred from the bias stress and those variations limit the application of IGZO TFTs in display applications such as active matrix organic light emitting diodes (AMOLED) resulting in the non-uniform pixel brightness [6]. For commercialization, understanding the electrical instability of IGZO TFTs is important. Although several papers reported the electrical instability of IGZO TFTs [6–10], they did not consider the effects of channel layer thickness on electrical instability of IGZO TFTs. In this paper, the bias stress-induced instability of IGZO TFTs with the variations of channel layer thickness is reported. Positive gate bias ($V_{GS}$) stresses were applied to IGZO TFTs with the different channel layer thickness. The stretched-exponential model for $V_{th}$ shift ($\Delta V_{th}$) as a function of stress time is used to analyze the effect of the channel layer thickness variation on the tested TFTs.

2. Experimental and stress conditions

The tested IGZO TFTs in this work were fabricated on conventional staggered bottom gate structure [11,12]. The test structures were fabricated on a glass substrate with 250-nm Mo gate metal deposited by sputtering. The 200-nm SiN$_d$ layer was then deposited as a gate insulator by plasma enhanced chemical vapor deposition (PECVD). The IGZO channel were deposited by sputtering using a polycrystalline In$_2$Ga$_2$ZnO$_7$ (In$_2$O$_3$:Ga$_2$O$_3$:ZnO = 1:1:1 mol%) target [11,12] with thicknesses of 40, 50, and 60 nm. The atomic ratio of the IGZO channel was In:Ga:Zn = 2.2:2.2:1 [12]. Finally, the source and drain electrodes were deposited via sputtering and patterned via photolithography and wet etching. The channel width ($W$) and length ($L$) of the TFTs were 50 $\mu$m and 25 $\mu$m, respectively. The current–voltage ($I$–$V$) of the TFTs was measured at room temperature using a Keithley 236 source measure unit. $V_{GS}$ stresses of 10, 20, and 30 V for 10$^4$ s with the grounded drain and source electrodes were applied to test electrical instability of the IGZO TFTs. The transfer characteristics ($I_{DS}$–$V_{GS}$) were measured between stress steps to extract stress-induced $\Delta V_{th}$ as a function of stress time. $I_{DS}$–$V_{GS}$ curve was measured in the $V_{GS}$ range of −5 to 15 V with drain voltage ($V_{DS}$) of 2.1 V. The $\Delta V_{th}$ is defined as the difference between $V_{th}$ value at the time and the initial $V_{th}$ value. Each $V_{th}$ was extracted by

* Corresponding author. Tel.: +82 2 2123 4619; fax: +82 2 313 2879.
E-mail address: iyun@yonsei.ac.kr (I. Yun).

© 2011 Elsevier Ltd. All rights reserved.

0026-2714/$$ - see front matter © 2011 Elsevier Ltd. All rights reserved.
linear extrapolation of $I_{DS}-V_{GS}$ curve in the range of 90–10% of the maximum $I_{DS}$ [7].

3. Results and discussion

3.1. Initial electrical characteristics

In order to investigate the electrical instability of the IGZO TFTs, the initial electrical characteristics of the TFTs are measured. For the initial electrical characteristics, four tested TFTs are measured with each channel layer thickness of 40, 50, and 60 nm. Fig. 1 shows the representative initial electrical characteristics when the channel layer thicknesses are 40, 50, and 60 nm, respectively. $V_{th}$ and the subthreshold swing ($S_{SUB}$) are extracted from $I_{DS}-V_{GS}$ with respect to the channel layer thickness. The solid line represents the extracted $V_{th}$ and it is clearly observed that $V_{th}$ decreases as the channel layer thickness increases. Similar results were reported previously such as ZnO TFTs [3], IZO TFTs [4], and IGZO TFTs [5]. The decrease of $V_{th}$ was commonly explained by the increase at number of free carriers as the channel layer thickness increases [4,5]. $S_{SUB}$ defined by $V_{GS}$ variation to increase $I_{DS}$ by a factor of 10, is determined by:

$$S_{SUB} = \frac{dV_{GS}}{d(\log I_{DS})}$$

Degradation of $S_{SUB}$ is observed as channel layer thickness increases which similar results were reported in the previous papers [4,5]. Fig. 2 shows the change of $V_{th}$ and $S_{SUB}$ as the channel layer thickness varies. Each error bar indicates the variation between the tested TFTs with the same channel layer thickness.

3.2. Positive gate bias stress

Fig. 3 shows the plots of linear $I_{DS}-V_{GS}$ stressed at $V_{GS}$ of 20 V when channel layer thicknesses are 40, 50, and 60 nm, respectively. The slope of curves does not much change despite of the increase of the bias stress time indicating that the change of mobility can be ignored [13]. The insets show the plots of $[\log(I_{DS})-V_{GS}]$ before and after $V_{GS}$ stresses. $S_{SUB}$ values are calculated as $\sim 0.26$ V/decade, $\sim 0.33$ V/decade, and $\sim 0.45$ V/decade when the channel layer thicknesses are 40, 50, and 60 nm, respectively. It is shown that each $I_{DS}-V_{GS}$ curve shifts to the positive direction as the stress time increases with no definite change of $S_{SUB}$. A lack of $S_{SUB}$ variation indicates carrier trapping in the channel/insulator interface or/and in the insulator bulk region [7] or/and in the deep acceptor-like traps of channel [9] with negligible creation of defect states. The positive $\Delta V_{th}$ is explained by trapping of carriers in the defect states. The trapped carriers screen the applied $V_{GS}$ resulting in a decrease of the effective $V_{GS}$ [13].

Fig. 4 shows the time dependence of $\Delta V_{th}$ under the constant $V_{GS}$ stress of 20 V with the variation of the channel layer thickness. The scattered points mean the measured $\Delta V_{th}$ values and the solid lines represent the stretched-exponential function for $\Delta V_{th}$. The stretched-exponential function has been developed for modeling $\Delta V_{th}$ by carrier trapping of a-Si:H TFTs [14]. The measured $\Delta V_{th}$ values well fit with the stretched-exponential function indicating that carriers are trapped with no creation of additional defect states which is also consistent with the lack of $S_{SUB}$ variation as the stress time increases. The stretched-exponential function for $\Delta V_{th}$ is described as [13,14]:

$$\Delta V_{th} = \Delta V_{th0}(1 - \exp(-t/\tau^\beta))$$

where $\Delta V_{th0}$ is $\Delta V_{th}$ at infinite time, $\beta$ is the stretched-exponential exponent, and $\tau$ is the characteristic trapping time of carriers. The solid line represents the stretched-exponential model and the stretched-exponential parameters are extracted. $\Delta V_{th0}$ increases from 3.6 V to 9.8 V as the channel layer thickness increases from 40 to 60 nm and $\beta$ is in the range of 0.39–0.53. The characteristic trapping time, $\tau$, is modeled as $\sim 10^4$ s. It is worth to note that $\tau$ values were previously reported as in the range of $1.8 \times 10^4$ and $5.8 \times 10^4$ s with thermally oxidized SiO$_2$ as a gate insulator [9,13]. Our modeled $\tau$ value is smaller than the previously reported $\tau$ values indicating that carrier trapping time is faster. Regarding that thermally oxidized SiO$_2$ is more stable than SiN$_x$ [9], it is reasonable that our modeled $\tau$ value is smaller than previously reported $\tau$ values. The modeled $\tau$ value shows almost the same for the tested TFTs with the different channel layer thicknesses. From the similar $\tau$, it can be assumed that the larger $\Delta V_{th}$ observed as the channel layer thickness increases results from the more number of trapped carriers not from the difference of the trapping time. As can be seen from the increase of the extracted $\Delta V_{th0}$ with the increase of the channel layer thickness, it is clearly shown that $\Delta V_{th}$ increases as the channel layer thickness increases. Fig. 5 shows the extracted $\Delta V_{th0}$ from the stretched-exponential function for various $V_{GS}$ stresses. For $V_{GS}$ stresses of 10 and 30 V, tendencies for the increase of $\Delta V_{th0}$ as the channel layer thickness increases are shown such as $V_{GS}$ stress of 20 V.

It should be clarified why $\Delta V_{th}$ increases as the channel layer thickness increases. It is worth to note that the density of total trap states ($N_t$) including the both density of deep bulk states in channel itself ($N_{bulk}$) and density of defects in channel/insulator...
interface ($N_{i_c}$) have relationship with $S_{SUB}$ value by the following relationship [15,16]:

$$N_{T} = N_{bulk} + N_{i_c} = \left(\frac{S_{SUB} \log(e)}{kT/q} - 1\right) \frac{C_{OX}}{q} \tag{3}$$

where $e$ is the Euler’s number (irrational constant), $k$ is the Boltzmann constant, $T$ is the absolute temperature, $q$ is the charge of an electron, and $C_{OX}$ is the gate insulator capacitance per unit area.

According to Eq. (3), the total trap states with the channel layer thickness of 40, 50, and 60 nm are extracted to be $7.11 \times 10^{11}$, $9.26 \times 10^{11}$, and $1.35 \times 10^{12}$ cm$^{-2}$, respectively. It is shown that $N_{T}$ increases as the channel layer thickness increases. Previously, the increase of $N_{T}$ was explained by assuming the constant channel layer trap density across the film [5]. If the channel layer trap density is constant, $N_{T}$ is proportional to the channel layer thickness, which leads to the increase of $N_{T}$ as the channel layer thickness increases. It is also shown that free carriers are increased as the channel layer thickness increases in the previous section. The increase of $\Delta V_{th}$ as the channel layer thickness increases can be thought as the combined effects of $N_{T}$ and free carriers. Assuming that the $\Delta V_{th}$ is due to the trapped carriers, $\Delta V_{th}$ can be expressed as [6,8]:

$$\Delta V_{th} = qN_{T}/C_{OX} \tag{4}$$

From Eq. (4), the increase of $N_{T}$ results in an increase of $\Delta V_{th}$. The rate at which the carriers are trapped depends on the free carriers [6,8]. The increase of $N_{T}$ makes more carriers being trapped and the increase of free carriers makes trapping rate higher.

4. Conclusion

Bias stress instability of the IGZO TFTs with the different channel layer thicknesses has been investigated with varying $V_{GS}$ stresses. The initial electrical characteristics of the TFTs showed smaller $V_{th}$ and larger $S_{SUB}$ as the channel layer thickness increased. From the $V_{GS}$ stress, the stretched-exponential model was well fitted with the experimentally measured $\Delta V_{th}$, which indicated that carriers were trapped in $N_{T}$ rather than the creation of the additional...
defect states. The $\Delta V_{th}$ showed an incremental trend as the channel layer thickness is increased which was thought to be attributed to the increase of $N_T$ and free carriers.

Acknowledgements

This work was supported by Yonsei University, Institute of TMS Information Technology, a Brain Korea 21 program, Korea. This work was also supported as a research project of Samsung Electronics.

References